Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A full depletion SOI-MOS transistor comprising:

a substrate having a main surface;

a buried oxide layer formed on the main surface of the substrate;

a thin silicon layer formed on the buried oxide layer, the thin silicon layer including a channel region and a source/drain region;

an isolation layer formed on the buried oxide layer, the isolation layer ~~surrounding~~ adjacent the thin silicon layer;

a gate insulation layer formed on the channel region of the thin silicon layer;

a gate electrode formed on the gate insulation layer; and

a polysilicon layer formed on the source/drain region of the thin silicon layer.

Claim 2 (Currently Amended): A full depletion SOI-MOS transistor according to claim 1, further comprising a sidewall formed on the gate insulation layer, ~~wherein the sidewall surrounds~~ adjacent the gate electrode.

Claim 3 (Original): A full depletion SOI-MOS transistor according to claim 1, wherein the polysilicon layer extends on the isolation layer.

Claim 4 (Original): A full depletion SOI-MOS transistor according to claim 2, wherein the polysilicon layer extends on the sidewall.

Claim 5 (Original): A full depletion SOI-MOS transistor according to claim 1, wherein a thickness of the thin silicon layer is about 20 to 80 percent of a total thickness of the thin silicon layer and the polysilicon layer.

Claim 6 (Currently Amended): A full depletion SOI-MOS transistor according to claim 1, wherein a thickness of the thin silicon layer is [[about]] less than about 35 nm.

Claim 7 (Currently Amended): A full depletion SOI-MOS transistor comprising:

a substrate having a main surface;

a buried oxide layer formed on the main surface of the substrate;

a thin silicon layer formed on the buried oxide layer, the thin silicon layer including a channel region and a source/drain region;

an isolation layer formed on the buried oxide layer, the isolation layer ~~surrounding~~ adjacent the thin silicon layer;

a gate insulation layer formed on the channel region of the thin silicon layer;

a gate electrode formed on the gate insulation layer; and

a silicide layer formed directly on the source/drain region of the thin silicon layer and the gate electrode.

Claim 8 (Currently Amended): A full depletion SOI-MOS transistor according to claim 7, further comprising a sidewall formed on the gate insulation layer, ~~wherein the sidewall surrounds~~ adjacent the gate electrode and adjacent the silicide layer formed ~~thereon~~ on the gate electrode.

Claim 9 (Original): A full depletion SOI-MOS transistor according to claim 7, wherein the silicide layer formed on the source/drain region extends on the isolation layer.

Claim 10 (Original): A full depletion SOI-MOS transistor according to claim 8, wherein the silicide layer formed on the source/drain region extends on the sidewall.

Claim 11 (Original): A full depletion SOI-MOS transistor according to claim 7, wherein a thickness of the thin silicon layer is about 20 to 80 percent of a total thickness of the thin silicon layer and the silicide layer formed on the source/drain region.

Claim 12 (Currently Amended): A full depletion SOI-MOS transistor according to claim 7, wherein a thickness of the thin silicon layer is [[about]] less than about 35 nm.

Claim 13 (Currently Amended): A full depletion SOI-MOS transistor comprising:

a substrate having a main surface;

a BOX layer formed on the main surface of the substrate;

an SOI layer formed on the BOX layer, the SOI layer including a channel region and a source/drain region;

an isolation layer formed on the BOX layer, the isolation layer ~~surrounding~~ adjacent the SOI layer;

a gate insulation layer formed on the channel region of the SOI layer;

a gate electrode formed on the gate insulation layer; and

a high mobility conductive layer formed on the source/drain region of the thin silicon layer, the high mobility conductive layer containing polysilicon.

Claim 14 (Currently Amended): A full depletion SOI-MOS transistor according to claim 13, further comprising a sidewall formed on the gate insulation layer, ~~wherein the sidewall surrounds~~ adjacent the gate electrode.

Claim 15 (Original): A full depletion SOI-MOS transistor according to claim 13, wherein the high mobility conductive layer extends on the isolation layer.

Claim 16 (Original): A full depletion SOI-MOS transistor according to claim 14, wherein the high mobility conductive layer extends on the sidewall.

Claim 17 (Original): A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is about 20 to 80 percent of a total thickness of the SOI layer and the high mobility conductive layer.

Claim 18 (Currently Amended): A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is [[about]] less than about 35 nm.

Claim 19 (Original): A full depletion SOI-MOS transistor according to claim 13, wherein the high mobility conductive layer contains silicide.

Claim 20 (Original): A full depletion SOI-MOS transistor according to claim 19, wherein the high mobility conductive layer is formed on the gate electrode.